CLAIMS:

1. A method for accessing at least one memory unit based on an index vector comprising a plurality of values, said method comprising the steps of:

concurrently performing an operation on individual ones of said plurality of index vector values with a base value to generate a plurality of memory addresses; and

concurrently accessing individual ones of said plurality of memory addresses in said at least one memory unit.

2. The method of claim 1 wherein said operation is addition.

3. The method of claim 1 wherein said operation is bit replacement.

4. The method of claim 3 wherein said bit replacement operation is implemented with logical OR and a plurality of least significant bits of said base address are 0.

5. The method of claim 3 wherein said bit replacement operation is implemented with bit concatenation.

6. The method of claim 1 wherein said at least one memory unit comprises one multiport memory unit and wherein said step of concurrently accessing comprises the step of accessing individual ones of said plurality of memory addresses via one corresponding memory port.

7. The method of claim 1 wherein said at least one memory unit comprises a plurality of memory units and wherein said step of concurrently accessing comprises the step of accessing individual ones of said plurality of memory addresses in one corresponding memory unit.

8. The method of claim 1 wherein said step of concurrently accessing further comprises the steps of:

concurrently reading data from individual ones of said plurality of memory addresses; and

storing said data in a storage register.

9. The method of claim 1 wherein said step of concurrently accessing further comprises the step of concurrently writing data to individual ones of said plurality of memory addresses.

10. A method for accessing at least one memory unit based on an index vector comprising a plurality of segments, said method comprising the steps of:

concurrently performing an operation on a value stored in individual ones of said index vector segments with a base value to generate a first plurality of memory addresses;

adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address; and

concurrently accessing in said at least one memory unit either said first plurality of memory addresses or said single memory address.

11. The method of claim 10 wherein whether said first plurality of memory addresses or said single memory address is accessed is based on a mode select signal.

12. The method of claim 11 wherein said mode select signal is programmable.

13. The method of claim 10 wherein said operation is addition.

14. The method of claim 10 wherein said operation is bit replacement.

15. The method of claim 14 wherein said bit replacement operation is implemented with logical OR and a plurality of least significant bits of said base address are 0.

16. The method of claim 14 wherein said bit replacement operation is implemented with bit concatenation.

17. The method of claim 10 wherein said at least one memory unit comprises one multiport memory unit and wherein said step of concurrently accessing comprises the step of accessing either i) individual ones of said first plurality of memory addresses in a corresponding port of said multiport memory unit or ii) said single memory address in individual ones of said ports of said multiport memory unit.

18. The method of claim 10 wherein said at least one memory unit comprises a plurality of memory units and wherein said step of concurrently accessing comprises the step of accessing either i) individual ones of said first plurality of memory addresses in a corresponding one of said plurality of memory units or ii) said single memory address in individual ones of said plurality of memory units.

19. Apparatus comprising:

a first storage register for storing an index vector comprising a plurality of values;

a second storage register for storing a base value;

a plurality of operator circuits, individual ones of said plurality of operator circuits having a first input coupled to at least a portion of said first storage register and a second input coupled to said second storage register, said plurality of operator circuits for performing an operation on individual ones of said index vector values with said base value to generate a plurality of memory addresses on outputs of said operator circuits; and

at least one memory unit coupled to the outputs of said operator circuits such that said plurality of memory addresses are accessible in said at least one memory unit.

20. The apparatus of claim 19 wherein said operator circuits are adders.

21. The apparatus of claim 19 wherein said operator circuits are bit replacement circuits.

22. The apparatus of claim 21 wherein said bit replacement circuits are logical OR circuits and a plurality of least significant bits of said base address are 0.

23. The apparatus of claim 21 wherein said bit replacement circuits are bit concatenation circuits.

24. The apparatus of claim 19 wherein said at least one memory unit is a multiport memory unit and wherein individual ones of said ports of said multiport memory unit are coupled to an output port of a corresponding operator circuit.

25. The apparatus of claim 19 wherein said at least one memory unit comprises a plurality of memory units and wherein individual ones of said plurality of memory units is coupled to an output of a corresponding operator circuit.

26. Apparatus comprising:

a first storage register for storing an index vector comprising a plurality of segments;

a second storage register for storing a base value;

a plurality of operator circuits, individual ones of said plurality of operator circuits having a first input coupled to at least a portion of said first storage register and a second input coupled to said second storage register, said plurality of operator circuits for performing an operation on a value stored in individual ones of said index vector segments with said base value to generate a first plurality of memory addresses on outputs of said operator circuits;

an adder circuit having a first input coupled to said second storage register and a second input coupled to said first storage register for adding said base value to a value represented by the concatenation of said plurality of segments of said index vector to generate a single memory address;

a plurality of multiplexers, individual ones of said plurality of multiplexers having as a first input one of said first plurality of memory addresses generated by said operator circuits and as a second input said single memory address and as a third input a mode select signal such that said plurality of multiplexers outputs either said one of said first plurality of memory addresses or said single memory address on an output port depending on said mode select signal; and

at least one memory unit coupled to said output port of said multiplexers such that either said plurality of memory addresses or said single memory address is accessible in said at least one memory unit.

27. The apparatus of claim 26 wherein said operator circuits are adders.

28. The apparatus of claim 26 wherein said operator circuits are bit replacement circuits.

29. The apparatus of claim 28 wherein said bit replacement circuits are logical OR circuits and a plurality of least significant bits of said base address are 0.

30. The apparatus of claim 28 wherein said bit replacement circuits are bit concatenation circuits.

31. The apparatus of claim 26 wherein said at least one memory unit is a multiport memory unit and wherein individual ones of said ports of said multiport memory unit are coupled to an output port of a corresponding multiplexer.

32. The apparatus of claim 26 wherein said at least one memory unit comprises a plurality of memory units and wherein individual ones of said plurality of memory units is coupled to an output of a corresponding multiplexer.